P4C214
ULTRA HIGH-SPEED
16K x 16 LATCHED RAM

FEATURES

- Pin Compatible with the Popular 2x4Kx16 I386 Cache RAM
- Supports Processor Speeds up to 50 MHz
- Easily Configurable
  Direct Map   16Kx16
  Two-Way Set   2x8Kx16
- On-chip Address Latch
- Separate Lower & Upper Byte Select

- Single 5V ±10% Power Supply
- CMOS for Optimum Speed/Power
- Common Data I/O
- TTL Compatible Inputs & Outputs
- Three-State Outputs
- Package Options:
  52-pin PLCC and 52-pin Quad Cerpack

DESCRIPTION

The P4C214 is a 262,144-bit ultra high-speed CMOS cache SCRAM (Static CMOS Random Access Memory) with latched addresses. It is ideally suited for cache RAM applications with the MIPS PR3000A/PR3400, and Intel's 80386 and 80486 processors. It is pin programmable into either a 2x8Kx16 or 16Kx16 configuration.

The P4C214 is functionally and pin compatible with the popular 2x4Kx16 cache RAM while providing twice the density, thus allowing a very easy upgrade from 32K byte cache to 64K byte (or larger) cache.

A mode control pin (MODE) controls the configuration of the memory. When this pin is LOW, the SCRAM functions as a direct mapped 16Kx16-bit RAM with A12 having a faster addressing speed. When the MODE pin is HIGH, the

SCRAM functions as a two-way associative 2x8Kx16. In this mode, address bit A12 is not used and should be externally wired to ground. In either mode, the new higher-order address bit, A13, allows expanding the cache depth from 4K to 8K or from 8K to 16K in the same 52-pin footprint. Thus, two devices form a 64K byte cache; four devices form a 128 K byte cache, when used with an iX86.
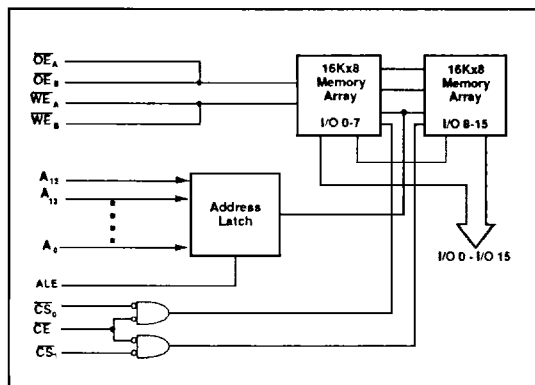
The P4C214 is manufactured using PACE III technology and is supported by a six-inch wafer fabrication production facility.

The P4C214 is available in a 52-pin PLCC and also in a 52-pin Quad Cerpack surface-mount package; each provides excellent board-level density.
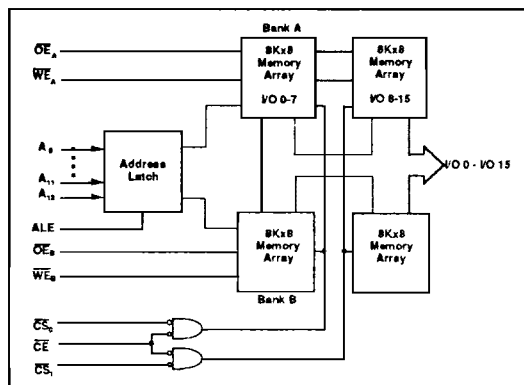
5

## DIRECT MAP (MODE = L)
## (For R3000 & iX86)

TWO-WAY SET (MODE = H)
(For iX86)

4/3/92

PIN DESCRIPTIONS

Pin Number(s)	Symbol	Type	Description
2, 3, 4, 5, 6, 7, 8, 34, 47, 48, 49, 50, 51	A_0–A_{11} A_{13}	Input	Address Inputs: These signals are latched on the negative edge of ALE.
46	A_{12}	Input	Fast Latched Address Input: This address is latched on the negative edge of ALE. Used in direct mode only. **_Must be GND for 2-way mode._**
52	ALE	Input	Address Latch Enable: When ALE is high, the latch is transparent. The negative edge latches the current address inputs (A_0–A_{13}).
45	$\overline{CE}$	Input	Chip Enable: To facilitate depth expansion.
23, 30	$\overline{CS_0},\overline{CS_1}$	Input	Byte Selects: These control signals control the lower and upper byte selection on the A or B side of the array. They also facilitate depth expansion.
28, 29	$\overline{OE_A},\overline{OE_B}$	Input	Output Enables: In the Two-Way Set Associative Mode, Active LOW enables cache bank A or B to drive the data bus. In the direct mode, these two pins must be wired together.
24, 25	$\overline{WE_B},\overline{WE_A}$	Input	Write Enables: These active LOW signals enable bank A or B. In the Two-Way Associative Mode, data may be written to bank A or B. In the direct mode, these two pins must be wired together.
11, 12, 13, 14, 16, 17, 18, 19, 35, 36 37, 38, 40, 41, 42, 43	I/O_0 - I/O_{15}	I/O	I/O: Data inputs and outputs.
1, 21, 22, 32, 33	Vcc	Supply Voltage	5V ±10%
9, 10, 15, 26, 27, 39, 44	GND	GND	Ground
31	MODE	Input	Configuration Control: When signal is LOW, the device functions as a direct map 16Kx16. When signal is HIGH, the device functions as a two-way associative 2x8Kx16.

3197 01

PIN CONFIGURATIONS
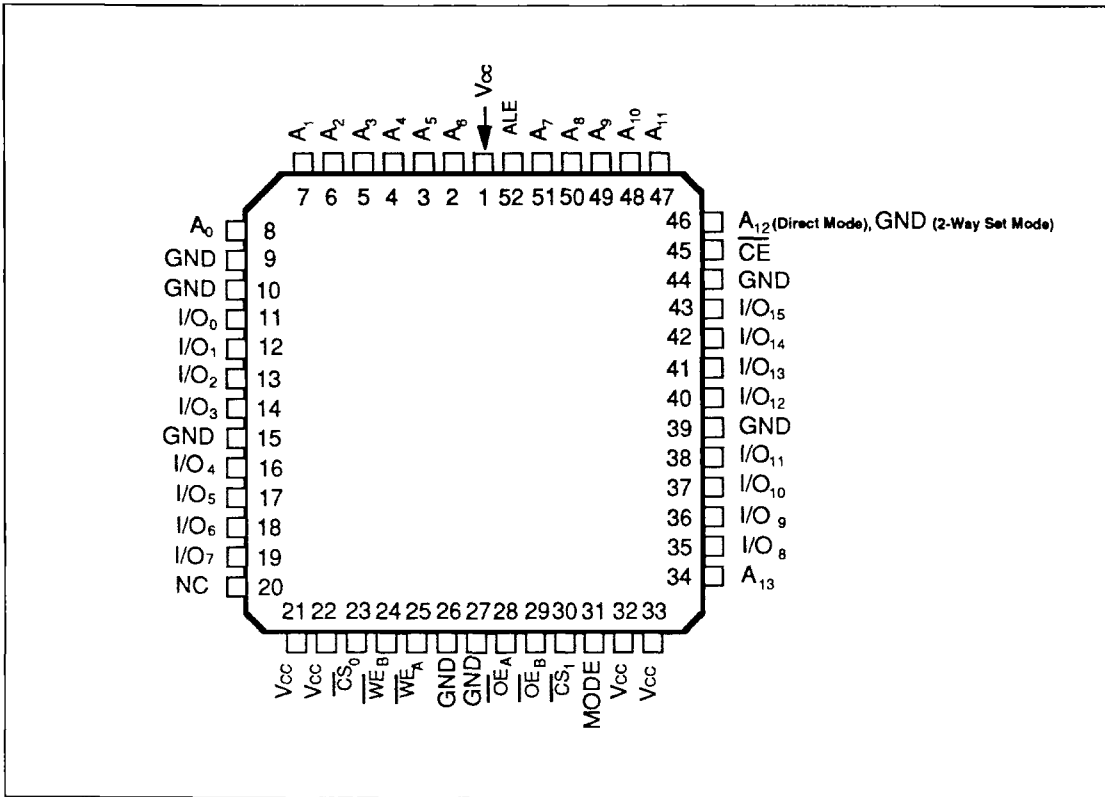
CACHE RAM CONFIGURATIONS FOR PR3000A AND i386/i486

MIPS PR3000A or PR3400 (64KB I- & d-Caches)

IX86 64K BYTE CACHE

4/3/92
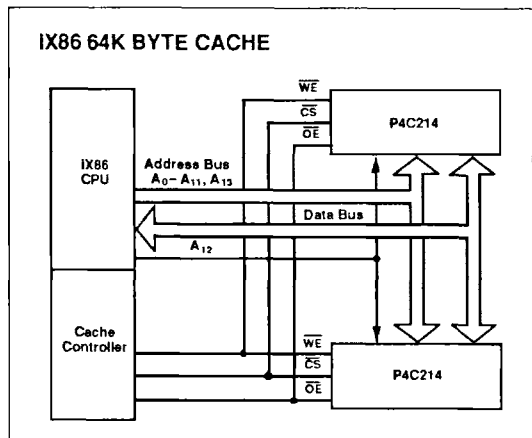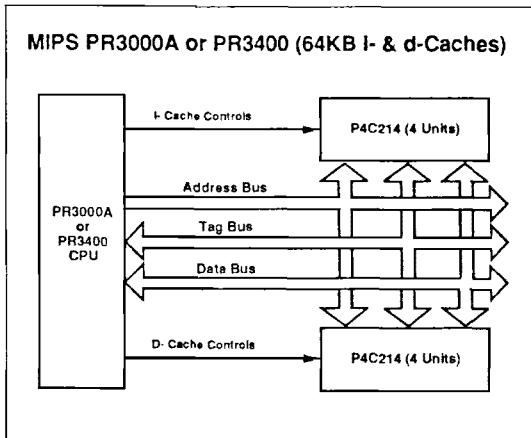
ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	−0.5 to +7.0	V
$V_{I/O}$	DC Input Voltage Applied to Output in High-Z	−0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	1.5	W
T_{OPR}	Operating Temperature	−55 to +125	°C

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−65 to +150	°C

3197 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	−55 to +125°C	0V	5.0V ± 10%

3197 09

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

3197 03

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage

Symbol	Parameter	Test Conditions	P4C214 Min	P4C214 Max	Unit
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage		−0.5[2]	0.8	V
I_{LI}	Input Leakage Current	$GND < V_{IN} < V_{CC}$	−10	+10	µA
I_{LO}	Output Leakage Current	$GND < V_O < V_{CC}$, Output Disabled	−10	+10	µA
I_{CC}	VCC Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, f = max (Note 4)		360	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4 mA	2.4		V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., I_{OUT} = GND		−350	mA

3197 04

CAPACITANCES[3]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

3197 05

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.

2. Transient inputs with V_{IL} & I_{IL} not more negative than −3.0V and −100mA, respectively, are permissible for pulse widths up to 20 ns.

3. This parameter is sampled and not 100% tested.

4. I_{CC} is measured with input levels at 0.0V and 3.0V except $\overline{OE}_A$ & $\overline{OE}_B$ ≥ 3.0V.

AC ELECTRICAL CHARACTERISTICS – READ CYCLE
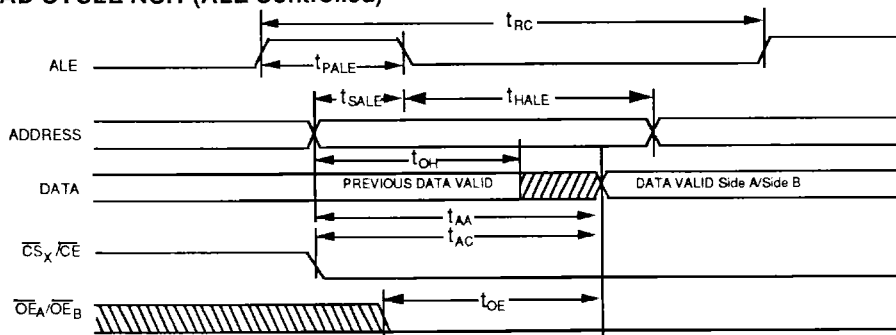### (Vcc = 5V ±10%, All Temperature Ranges)

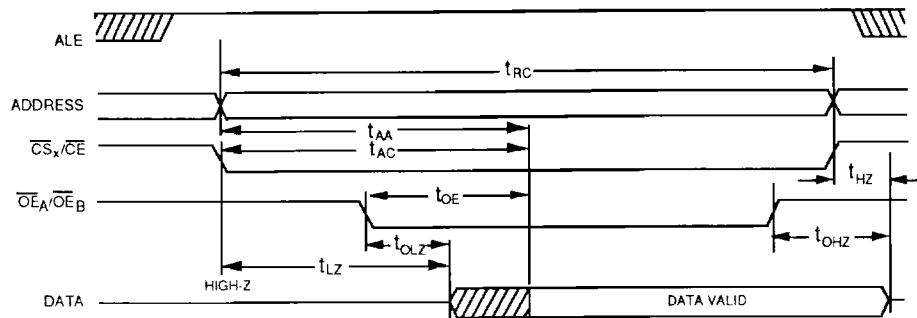| Sym	Parameter	-13		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	13		17		20		25		35		ns
t_{AA}	Address Access Time		13		17		20		25		35	ns
t_{AA12}	Fast Address Access Time		9		11		13		17		25	ns
t_{AC}	Chip Select Access Time		8		9		10		12		15	ns
t_{OE}	Output Enable to Output Valid		6		7		8		10		13	ns
t_{OH}	Output HOLD from address change	2		3		3		3		3		ns
t_{LZ}	Chip Enable to low-Z	2		2		3		3		3		ns
t_{OLZ}	Output Enable to low-Z	2		2		2		2		2		ns
t_{HZ}	Chip Enable to high-Z		9		10		12		15		25	ns
t_{OHZ}	Output Enable to high-Z		5		6		8		10		14	ns
t_{PALE}	ALE pulse width	6		6		6		8		10		ns
t_{SALE}	Address Setup to ALE Low	2		2		2		3		6		ns
t_{HALE}	Address Hold from ALE Low	2		2		2		2		4		ns

Notes: 1. t_{LZ}, t_{HZ}, t_{OLZ}, t_{OHZ} are measured ±200mV from Z-level.
2. Worst case for t_{OE} is when $\overline{OE}_A$ goes HIGH at the same time that $\overline{OE}_B$ goes LOW, and vice versa. However, such simultaneous switching does not occur in 2-way set associative or in direct mode cache applications.

READ CYCLE NO.1 (ALE Controlled)


READ CYCLE NO.2 (Address Controlled)

4/3/92

AC ELECTRICAL CHARACTERISTICS – WRITE CYCLE
(VCC= 5V ±10%, All Temperature Ranges)

Sym	Parameter	-13		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	13		17		20		25		35		ns
t_{AW}	Address Setup to End of Write	13		17		17		18		25		ns
t_{CW}	Chip Select to End of Write	13		17		17		18		25		ns
t_{DS}	Data Setup to End of Write	5.5		8		8		10		10		ns
t_{DH}	Data Hold from End of Write	0		0		0		0		0		ns
t_{WP}	Write Enable Pulse Width	8		12		15		18		25		ns
t_{AS}	Address Setup to Write Enable	0		0		0		0		0		ns
t_{AH}	Address Hold from Write Enable	0		0		0		0		0		ns
t_{WLZ}	Write Enable High to Low-Z	2		2		2		3		3		ns
t_{WHZ}	Write Enable Low to High-Z		9		11		13		15		15	ns
t_{PALE}	ALE Pulse Width		6		6		6		8		10	ns

Note: t_{WLZ}, t_{WHZ} are measured ±200mV from Z-level.

WRITE CYCLE
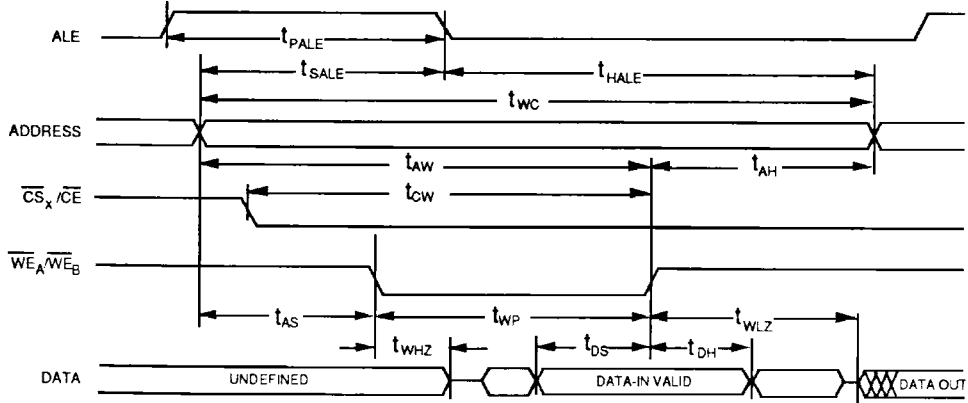
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 & 2

319700
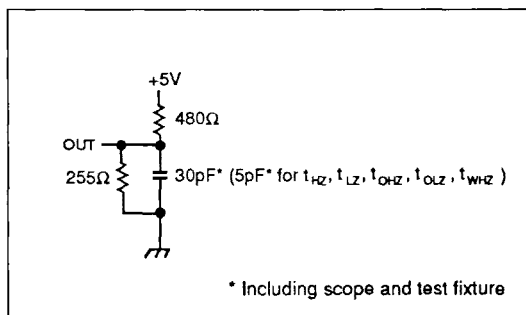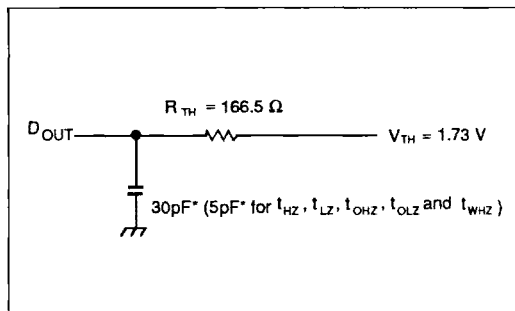

Figure 1. Output Load

Figure 2. Thevenin Equivalent

5

* Including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C214, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{cc} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V_{cc} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

TRUTH TABLES

TWO-WAY SET, 2X8KX16 (MODE = HIGH)

Mode		$\overline{CE}$	$\overline{CS}_0$	$\overline{CS}_1$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	I/O
Standby		H	X	X	X	X	X	X	High Z
		L	H	H	X	X	X	X	High Z
Output Disabled		X	X	X	H	H	X	X	High Z
		X	X	X	L	L	X	X	High Z
Read I/O_0 — I/O_7	Bank A	L	L	H	L	H	H	H	D_{OUT}
Read I/O_0 — I/O_7	Bank B	L	L	H	H	L	H	H	D_{OUT}
Read I/O_8 — I/O_{15}	Bank A	L	H	L	L	H	H	H	D_{OUT}
Read I/O_8 — I/O_{15}	Bank B	L	H	L	H	L	H	H	D_{OUT}
Read I/O_0 — I/O_{15}	Bank A	L	L	L	L	H	H	H	D_{OUT}
Read I/O_0 — I/O_{15}	Bank B	L	L	L	H	L	H	H	D_{OUT}
Write I/O_0 — I/O_7	Bank A	L	L	H	X	X	L	H	D_{in}
Write I/O_0 — I/O_7	Bank B	L	L	H	X	X	H	L	D_{in}
Write I/O_8 — I/O_{15}	Bank A	L	H	L	X	X	L	H	D_{in}
Write I/O_8 — I/O_{15}	Bank B	L	H	L	X	X	H	L	D_{in}
Write I/O_0 — I/O_{15}	Bank A	L	L	L	X	X	L	H	D_{IN}
Write I/O_0 — I/O_{15}	Bank B	L	L	L	X	X	H	L	D_{IN}
Write I/O_0 — I/O_7	Bank A & B	L	L	H	X	X	L	L	D_{IN}
Write I/O_8 — I/O_{15}	Bank A & B	L	H	L	X	X	L	L	D_{IN}
Write I/O_0 — I/O_{15}	Bank A & B	L	L	L	X	X	L	L	D_{IN}

DIRECT MAP, 16KX16 (MODE = LOW)

Mode	$\overline{CE}$	$\overline{CS}_0$	$\overline{CS}_1$	$\overline{OE}_A/\overline{OE}_B$	$\overline{WE}_A/\overline{WE}_B$	I/O
Standby	H	X	X	X	X	High Z
	L	H	H	X	X	High Z
Output Disabled	X	X	X	H	X	High Z
Read I/O_0 — I/O_7	L	L	H	L	H	D_{OUT}
Read I/O_8 — I/O_{15}	L	H	L	L	H	D_{OUT}
Read I/O_0 — I/O_{15}	L	L	L	L	H	D_{OUT}
Write I/O_0 — I/O_7	L	L	H	X	L	D_{IN}
Write I/O_8 — I/O_{15}	L	H	L	X	L	D_{IN}
Write I/O_0 — I/O_{15}	L	L	L	X	L	D_{IN}

Note: 1. $\overline{CE}$, when taken inactive while $\overline{WE}_A$ or $\overline{WE}_B$ remain active, allows a chip enable controlled write to be performed.
2. X = H or L

PACKAGE SUFFIX

Package Suffix	Description
PP	Plastic Leaded Chip Carrier (PLCC)
GR	Quad Cerpak (J-Bend Leads)

3187 10

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
B	–55°C to +125°C with MIL-STD-883D Class B compliance

3187 11

SELECTION GUIDE

The P4C214 is available in the following temperature, speed and package options.

Temperature Range	Package	13ns	17ns	20ns	25ns	35ns
Commercial	PLCC	-13 PP52C	-17 PP52C	-20 PP52C	-25 PP52C	-35 PP52C
Military Processed*	Quad CERPAK	N/A	N/A	N/A	-25 GR52B	-35 GR52B

3187 12

* Military temperature range with MIL-STD-883 Revision D, Class B processing.
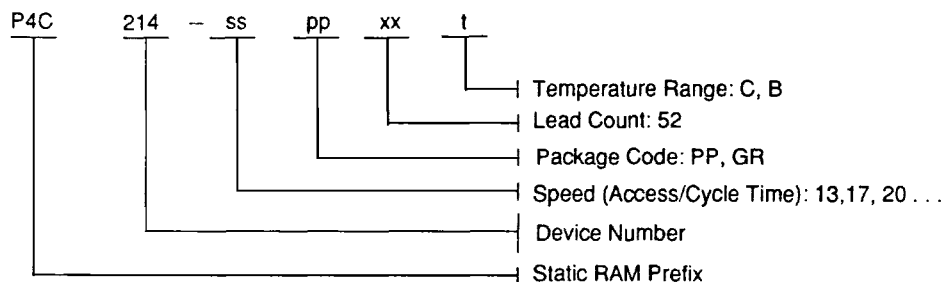 N/A = Not available

5

The P4C214 supports the high performance processor speeds of the i386 and i486, and the PR3000A/PR3400.

Processor	Frequency	Access Time	Output Enable	Performance Part Type
i386	40 MHz	20ns	8ns	P4C214 - 20
	33 MHz	25ns	10ns	P4C214 - 25
	25 MHz	35ns	13ns	P4C214 - 35
i486	50 MHz	14ns	7ns	P4C214 - 13
	33 MHz	19ns	8ns	P4C214 - 17
R3000	40 MHz	13ns	5ns	P4C214 - 13
	33 MHz	17ns	7ns	P4C214 - 17
	25 MHz	23ns	9ns	P4C214 - 20

3187 70

ORDERING INFORMATION

The following part numbering scheme is used for

```
P4C     214    --    ss     pp     xx     t
```

Temperature Range: C, B
Lead Count: 52
Package Code: PP, GR
Speed (Access/Cycle Time): 13, 17, 20 . . .
Device Number
Static RAM Prefix

1519 09